VERTICAL TRANSISTOR DEVICE STRUCTURE WITH CYLINDRICALLY-SHAPED REGIONS

REFERENCE TO RELATED APPLICATIONS

The present application claims priority to and the benefit of U.S. Provisional Patent Application Ser. No. 61/915,772, filed Dec. 13, 2013, entitled, "Vertical Transistor Device Structure With Cylindrically-Shaped Regions", the entirety of which is hereby incorporated by reference.

TECHNICAL FIELD

The present disclosure relates to semiconductor devices fabricated in a silicon substrate. More specifically, the present invention relates to vertical field-effect transistor device structures capable of withstanding high voltages.

BACKGROUND

High-voltage, field-effect transistors (HVFETs), also known as power transistors, are well known in the semiconductor arts. Most often, HVFETs comprise a vertical transistor device structure that includes an extended drain region that supports the applied high-voltage when the device is in the "off" state. HVFETs of this type are commonly used in power conversion applications such as AC/DC converters for offline power supplies, motor controls, and so on. These power transistor devices can be switched at high voltages and achieve a high blocking voltage in the "off" state while minimizing the resistance to current flow between the drain and source, often referred to as the specific on-resistance (Rds_{on}), in the "on" state.

BRIEF DESCRIPTION OF THE DRAWINGS

Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following figures, wherein like reference numerals refer to like parts throughout the various views unless otherwise specified.

FIG. **1** is a cross-sectional perspective view of an example vertical transistor device structure with cylindrically-shaped regions.

FIG. **2** is a top view of an example layout of the vertical transistor device structure shown in FIG. **1**.

FIG. **3**A is an example cross-sectional side view of one embodiment of the vertical transistor device structure layout shown in FIG. **2**, taken along cut lines A-A'.

FIG. **3**B is an example cross-sectional side view of another embodiment the vertical transistor device structure layout shown in FIG. **2**, taken along cut lines A-A'.

FIG. **4** is a cross-sectional side view of the embodiment of FIG. **3**A with a graph illustrating the electric field (E-field) distribution in various regions of the device.

FIGS. **5**A-**5**B illustrate simulation results showing the potential contours as a function of distance for an example vertical transistor device for different doping and voltage conditions.

Corresponding reference characters indicate corresponding components throughout the several views of the drawings. Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of various embodiments of the present invention. Also, common but well-understood elements that are useful or necessary in a commercially feasible embodiment are often not depicted in order to facilitate a less obstructed view of these various embodiments of the present invention.

DETAILED DESCRIPTION

In the following description numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one having ordinary skill in the art that the specific details need not be employed to practice the present invention. In other instances, well-known systems, devices, or methods have not been described in detail in order to avoid obscuring the present invention.

Reference throughout this specification to "one embodiment", "an embodiment", "one example" or "an example" means that a particular feature, structure or characteristic described in connection with the embodiment or example is included in at least one embodiment of the present invention. Thus, appearances of the phrases "in one embodiment", "in an embodiment", "one example" or "an example" in various places throughout this specification are not necessarily all referring to the same embodiment or example. Furthermore, the particular features, structures or characteristics may be combined in any suitable combinations and/or sub-combinations in one or more embodiments or examples. Particular features, structures or characteristics may be included in an integrated circuit, an electronic circuit, a combinational logic circuit, or other suitable components that provide the described functionality. In addition, it is appreciated that the figures provided herewith are for explanation purposes to persons ordinarily skilled in the art and that the drawings are not necessarily drawn to scale.

For purposes of this disclosure, "ground" or "ground potential" refers to a reference voltage or potential against which all other voltages or potentials of a circuit or integrated circuit (IC) are defined or measured.

A vertical power transistor device structure having cylindrically-shaped regions is described. The vertical power transistor device structure has a low specific on-state resistance and supports high voltage in the off-state. In other embodiments the same device structure and layout may be utilized to implement a variety of different devices, including P-N diodes, high voltage Schottky diodes, junction field-effect transistors (JFETs), insulated-gate bipolar transistors (IGBTs), and the like.

The high voltage vertical power transistors may utilize field plates that help to reshape the electric filed around a central semiconductor pillar or mesa and thus increase the breakdown voltage. The cylindrically-shaped structure of the different regions in a vertical power transistor device described in this application allows a compact size with an increased voltage ratings and an efficient utilization of the silicon volume.

FIG. **1** is an example cross-sectional perspective view of a vertical transistor device **100** with cylindrically-shaped regions. The vertical transistor device structure of FIG. **1** includes a plurality of cylindrically-shaped dielectric regions **130** (e.g., oxide) disposed in a semiconductor layer **105** (e.g., silicon), which in one embodiment comprises an n-type epitaxial layer. Centrally disposed within each region **130** (e.g., dielectric region of oxide), and fully insulated from semiconductor layer **105**, is a cylindrically-shaped conductive field plate member **150**, which in one embodiment comprises polysilicon. Note that the cylindrically-